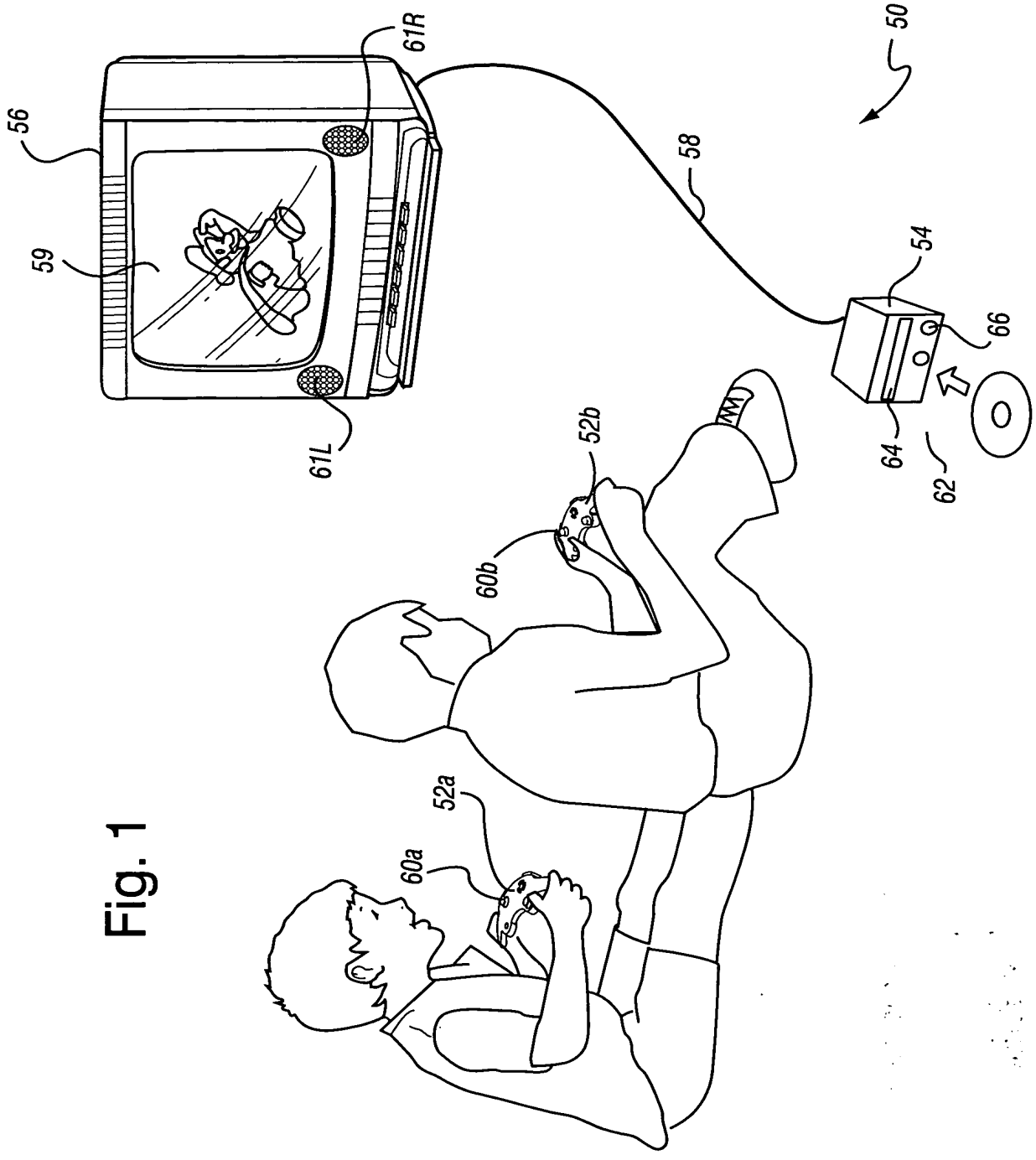


Fig. 1

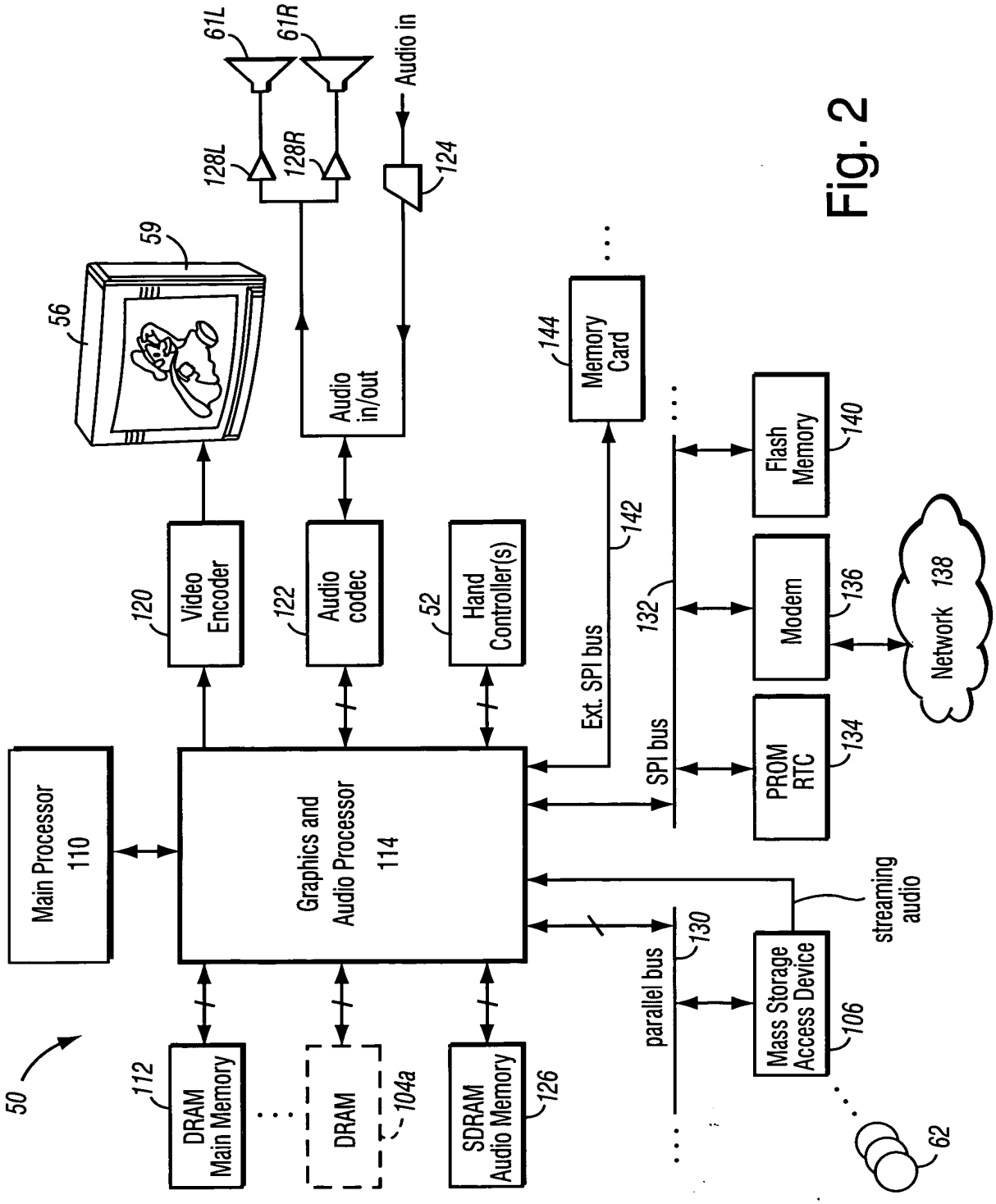


Fig. 2

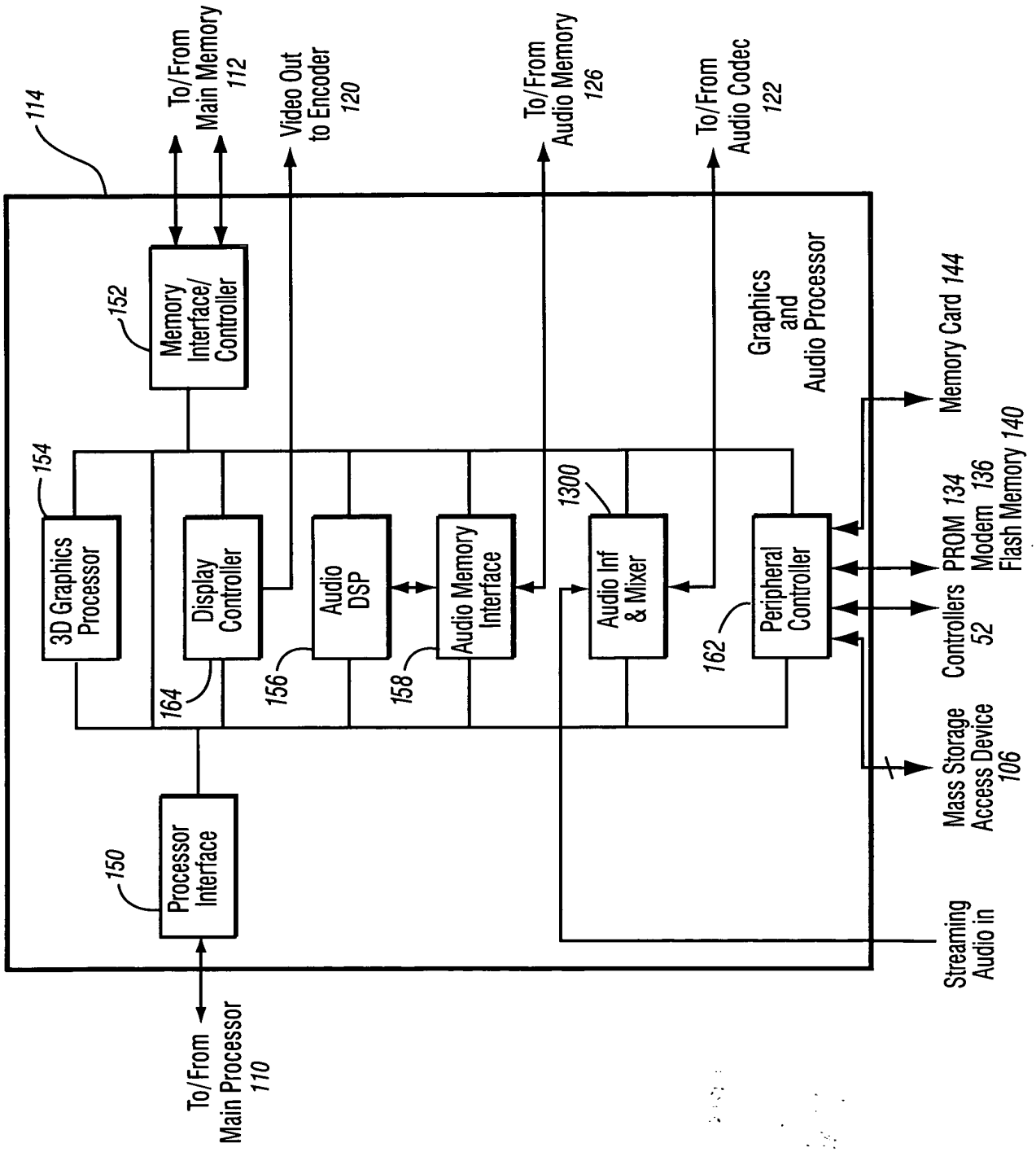


Fig. 3

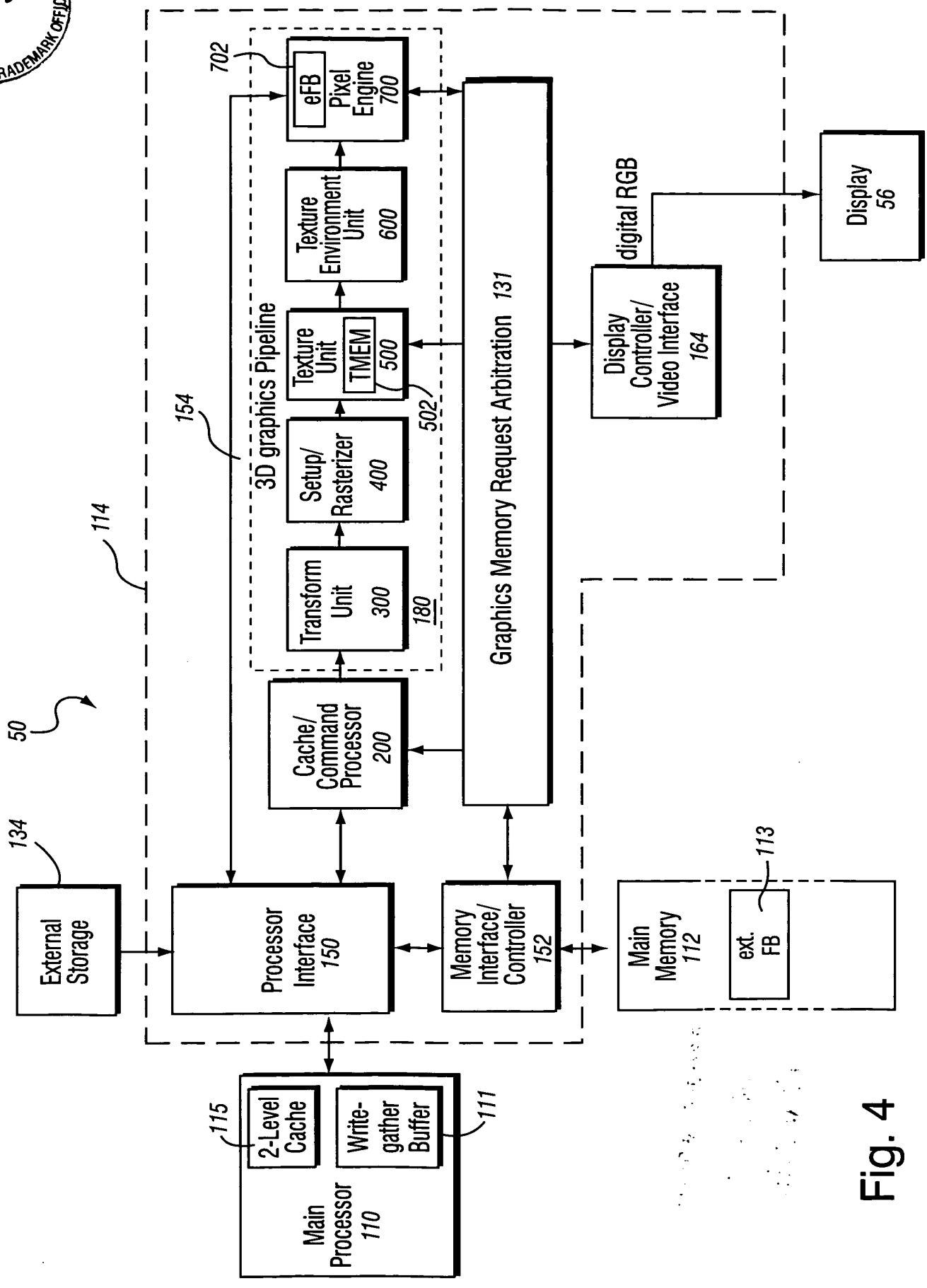


Fig. 4

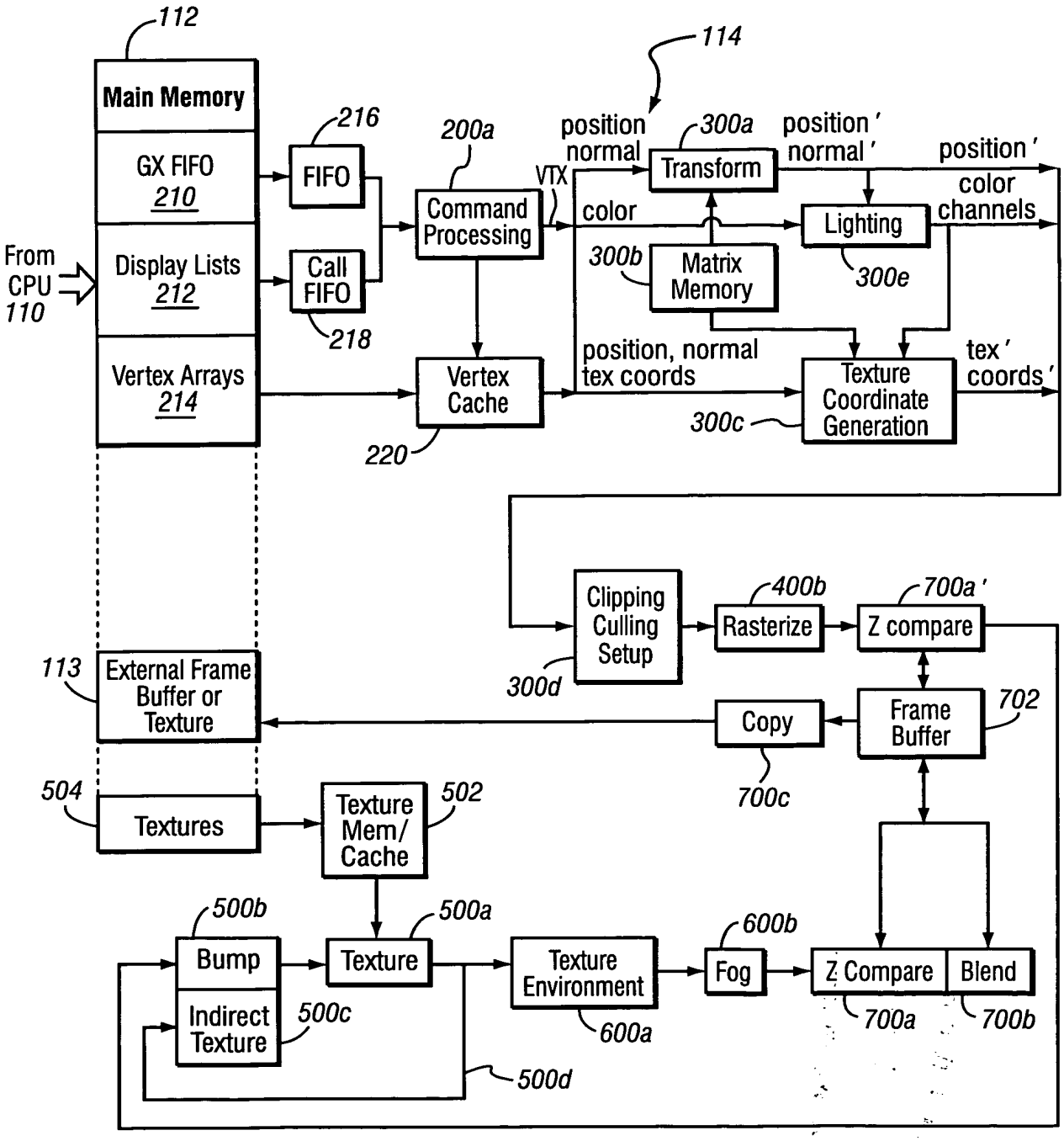
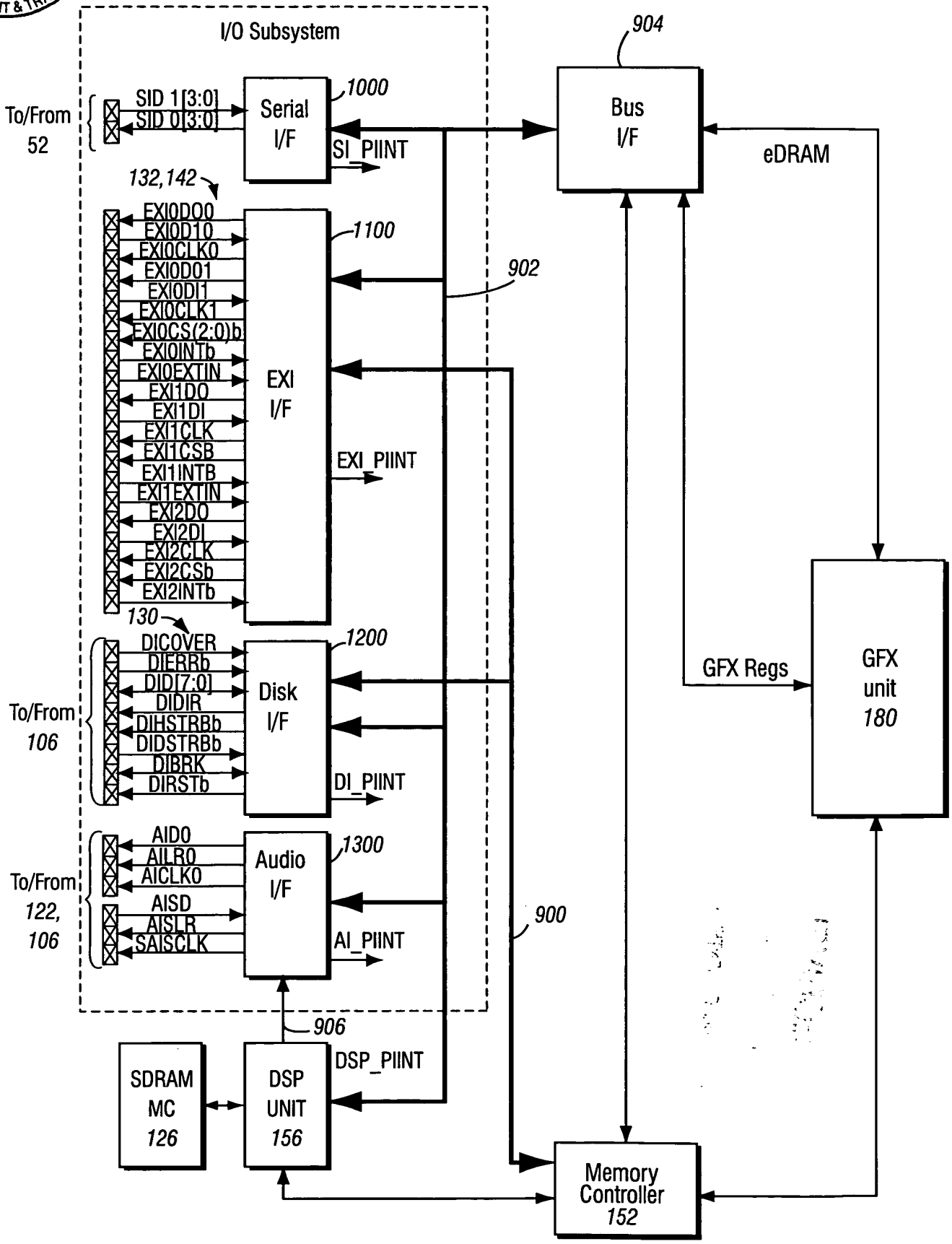


Fig. 5 EXAMPLE GRAPHICS PROCESSOR FLOW

Fig. 6 EXAMPLE INPUT/OUTPUT SUBSYSTEM



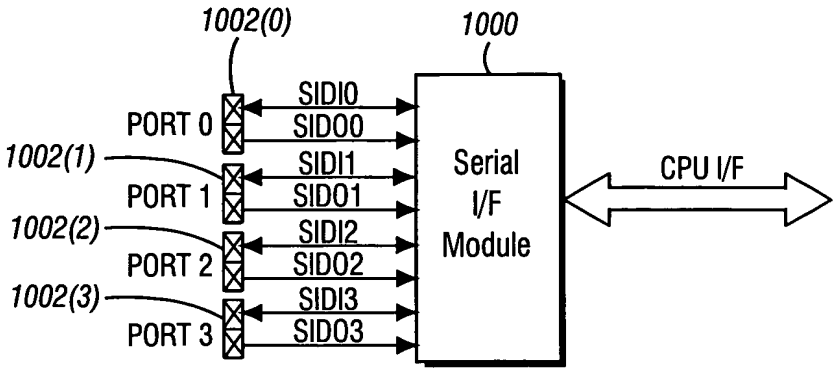


Fig. 7A
EXAMPLE SERIAL INTERFACE

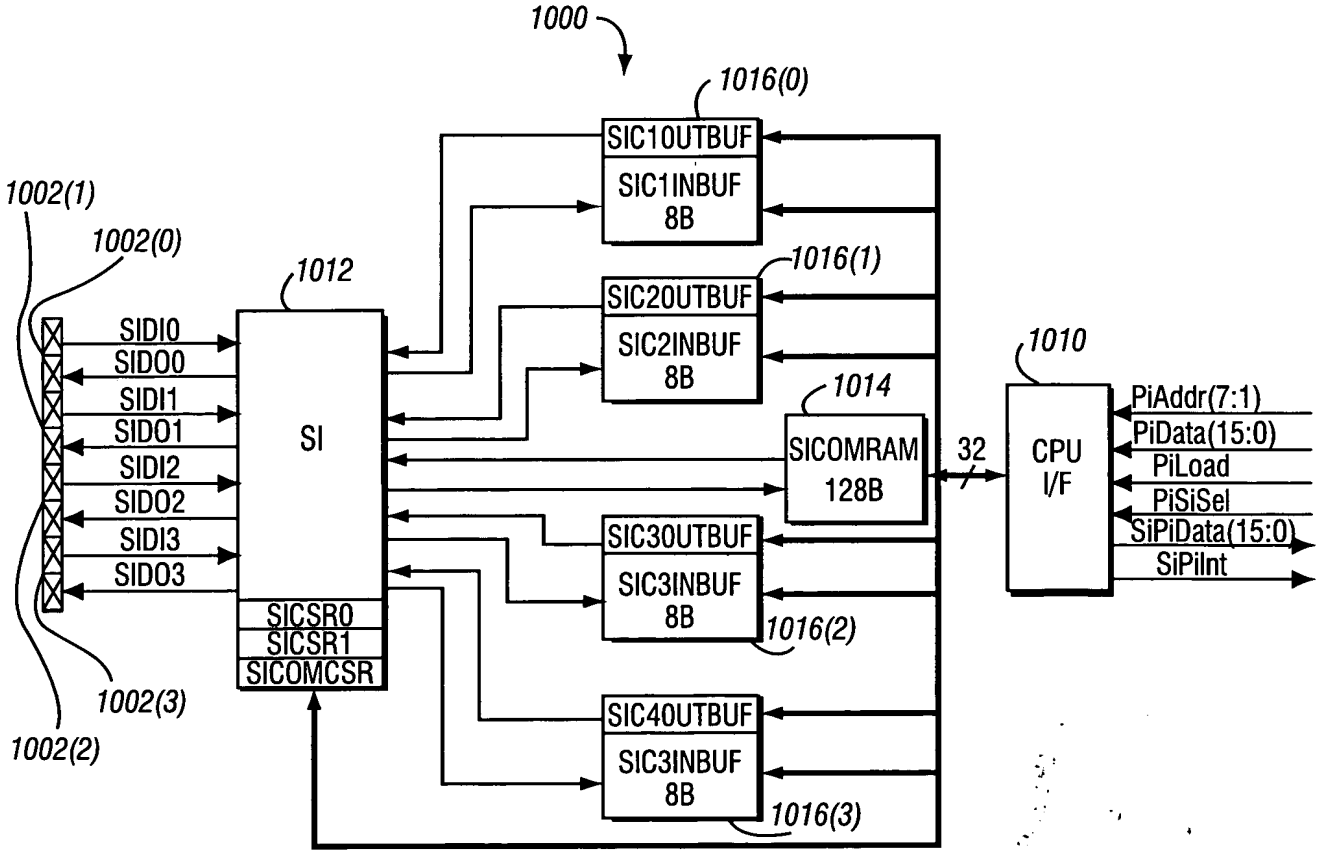


Fig. 7B
EXAMPLE SERIAL INTERFACE

Register				Offset(hex)
31	16	15	0	
SI Channel 0 Output Buffer (SIC0OUTBUF)				0x00
SI Channel 0 Input Buffer H (SIC0INBUFH)				0x04
SI Channel 0 Input Buffer L (SIC0INBUFL)				0x08
SI Channel 1 Output Buffer (SIC1OUTBUF)				0x0C
SI Channel 1 Input Buffer H (SIC1INBUFH)				0x10
SI Channel 1 Input Buffer L (SIC1INBUFL)				0x14
SI Channel 2 Output Buffer (SIC2OUTBUF)				0x18
SI Channel 2 Input Buffer H (SIC2INBUFH)				0x1C
SI Channel 2 Input Buffer L (SIC2INBUFL)				0x20
SI Channel 3 Output Buffer (SIC3OUTBUF)				0x24
SI Channel 3 Input Buffer H (SIC3INBUFH)				0x28
SI Channel 3 Input Buffer L (SIC3INBUFL)				0x2C
SI Poll Control Register (SIPOLL)				0x30
SI Communication Control Status Register (SICOMCSR)				0x34
SI Status Register (SISR)				0x38
SI EXI Lock Register (SIEXILK)				0x3C
SI Communication RAM (128 Bytes)				0x80-0xFF

Fig. 7C

EXAMPLE SERIAL INTERFACE REGISTERS

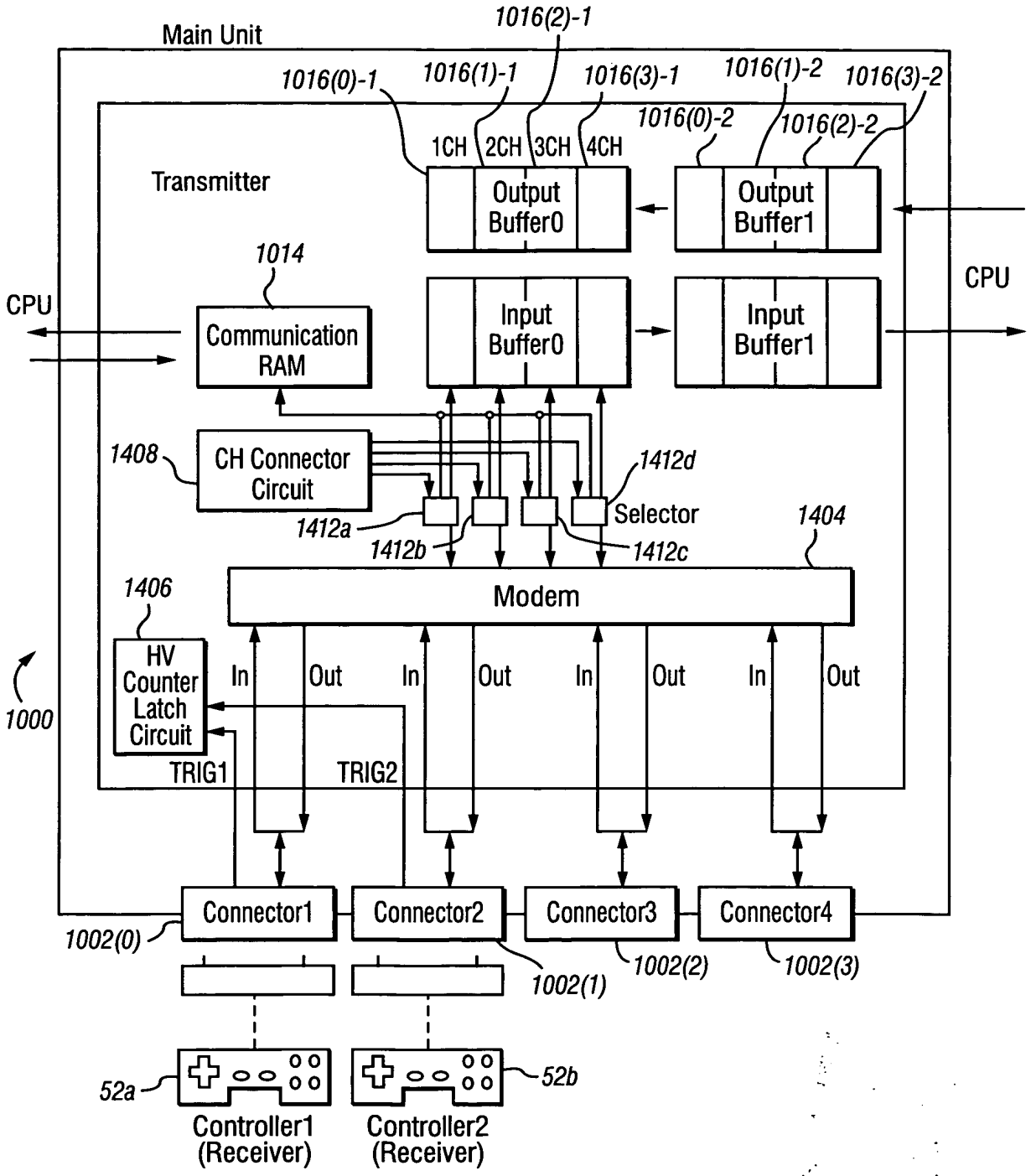


Fig. 8

EXAMPLE SERIAL INTERFACE

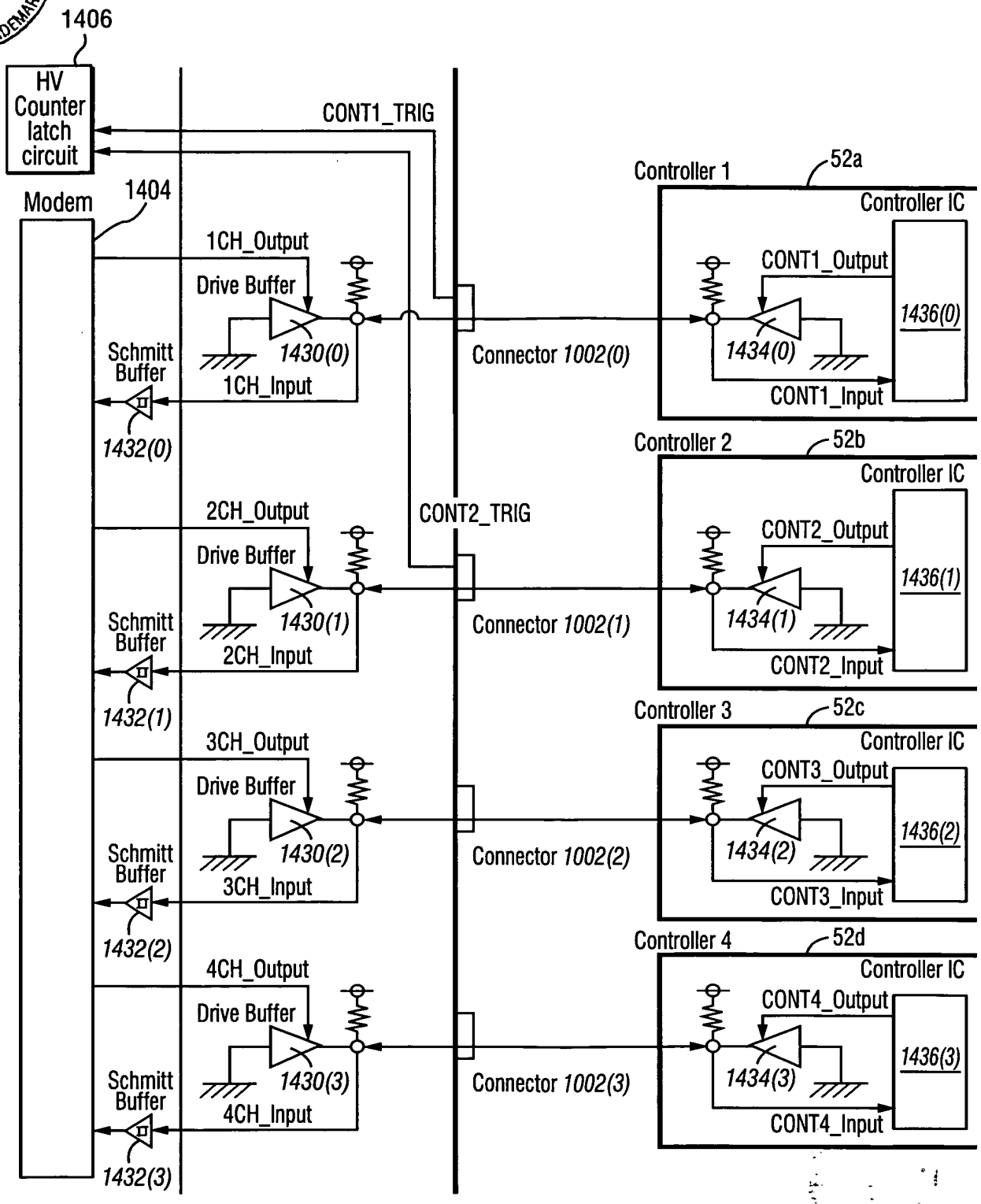


Fig. 9

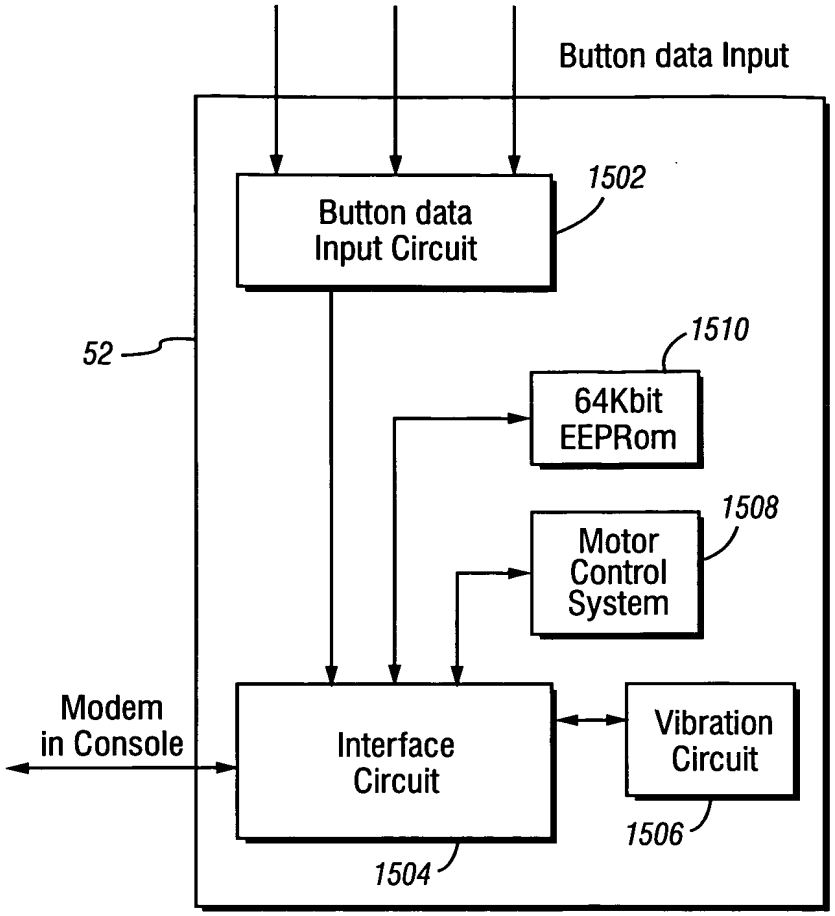


Fig. 10

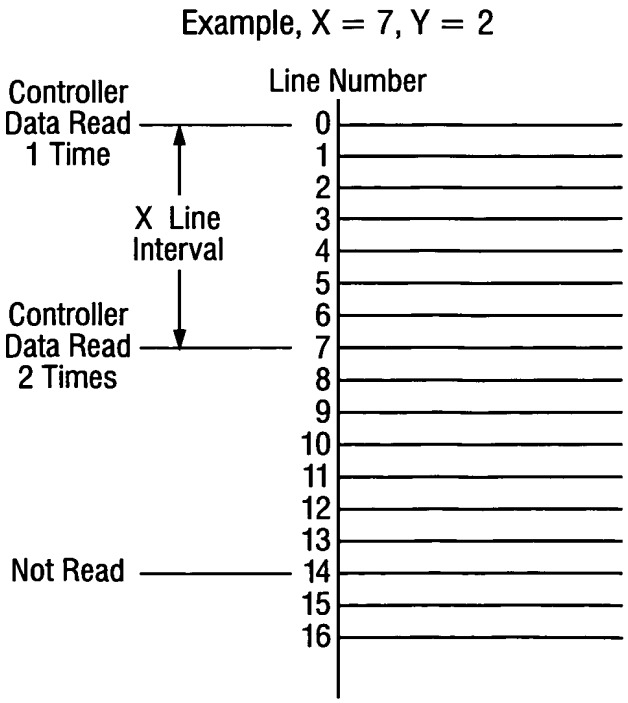


Fig. 12

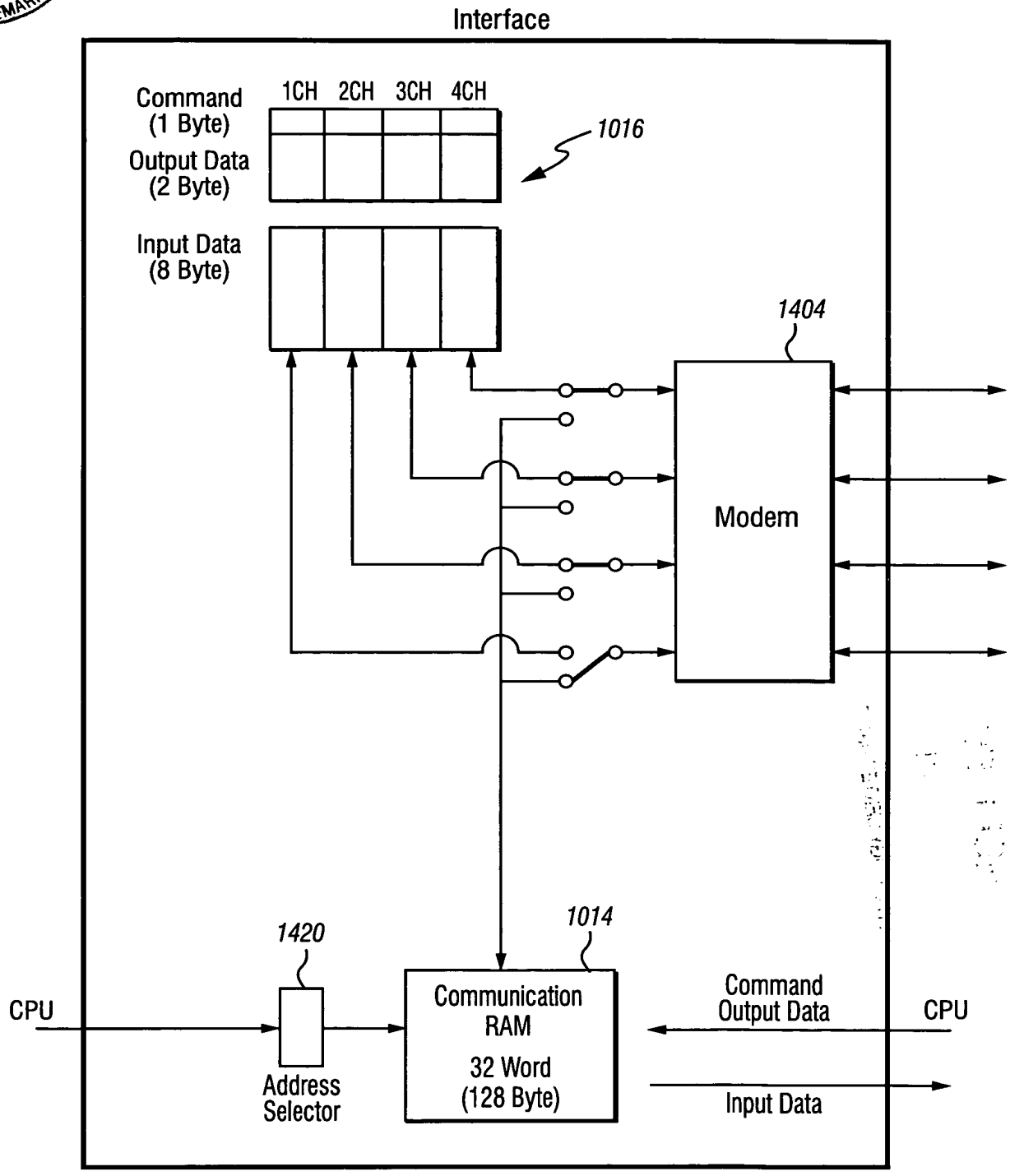


Fig. 11

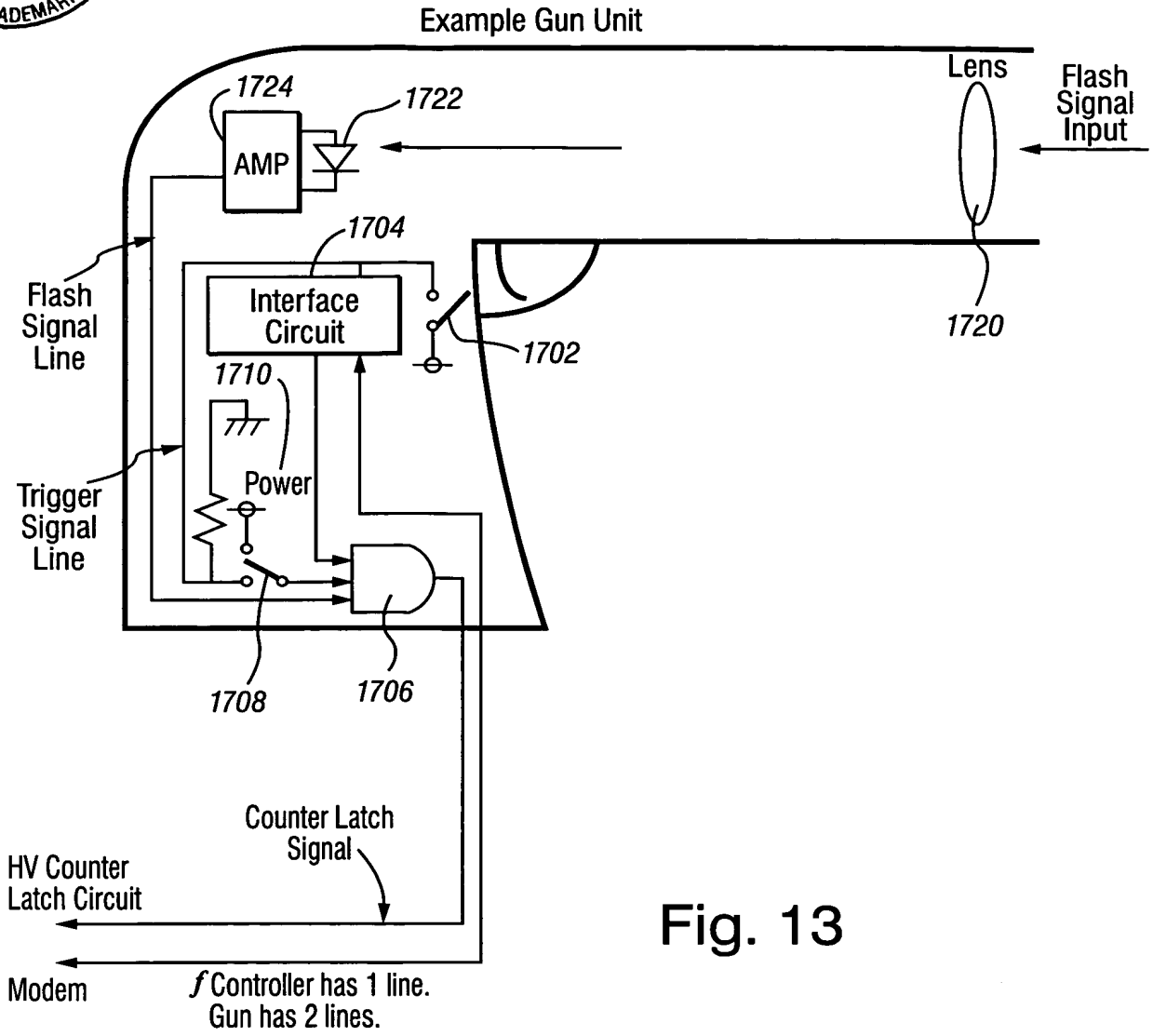


Fig. 13

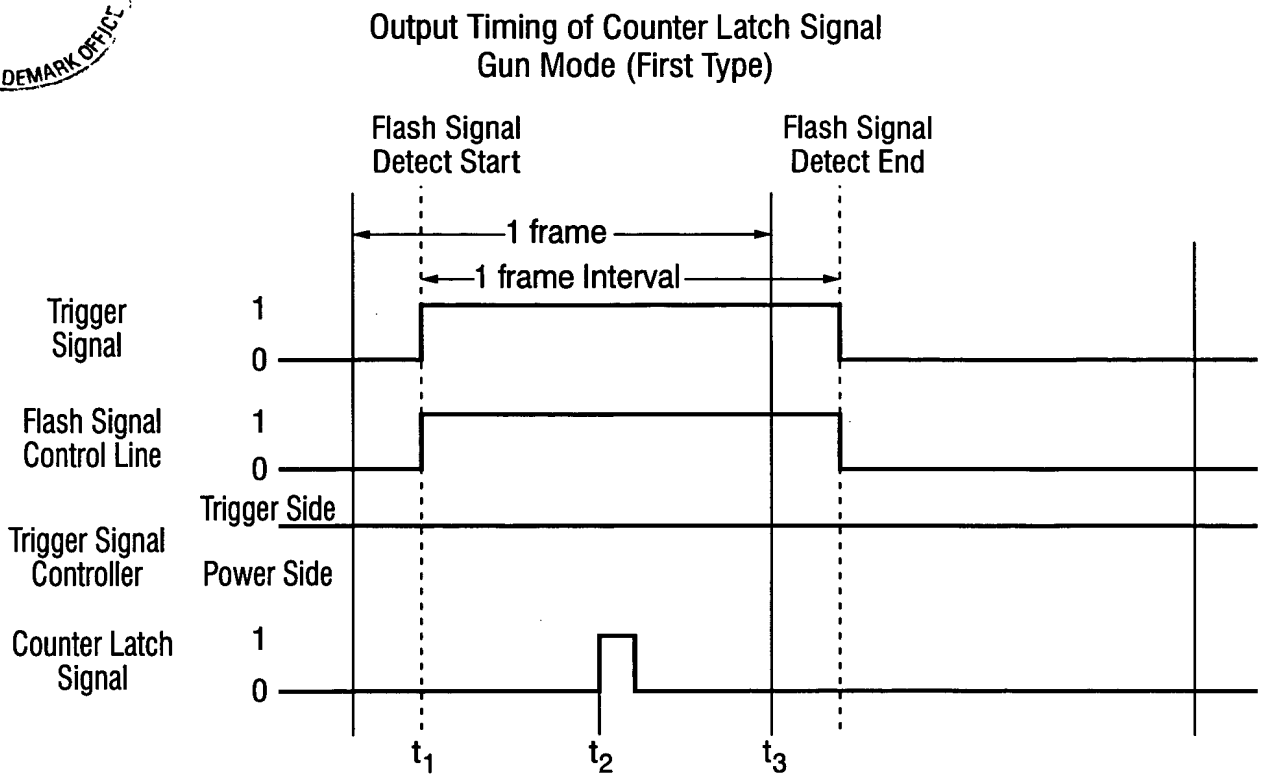


Fig. 14A

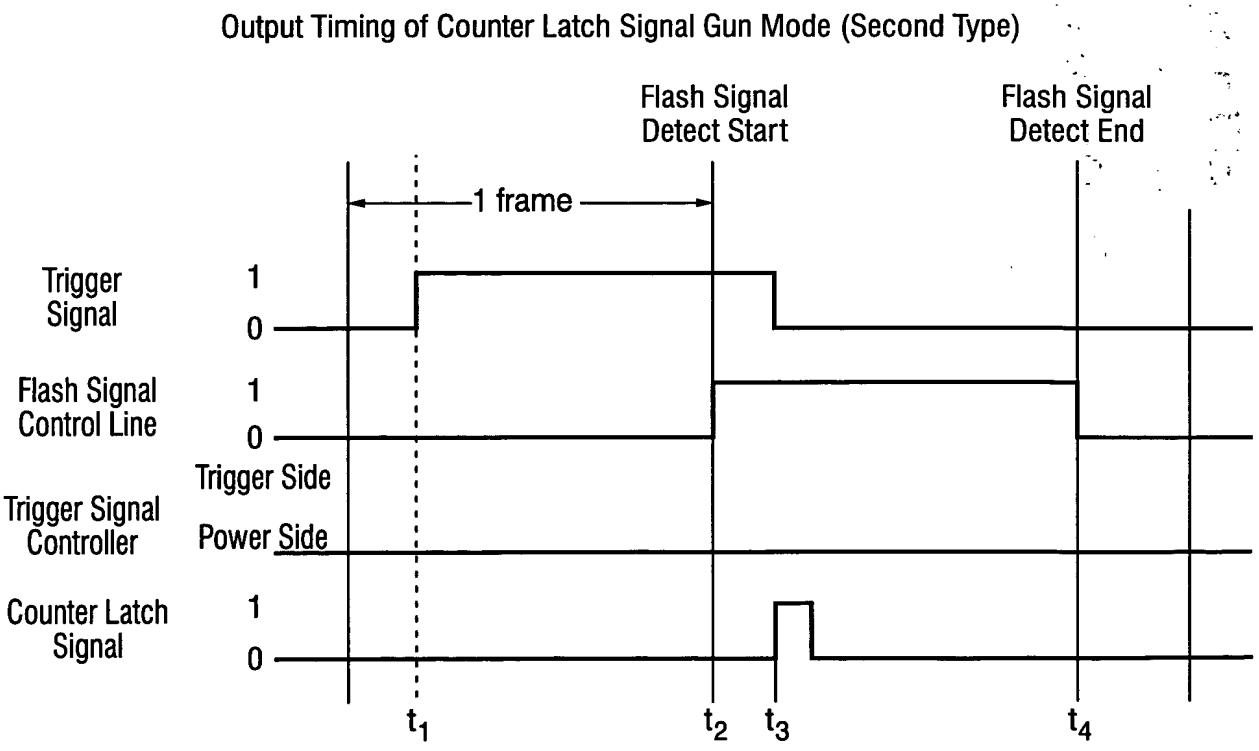


Fig. 14B

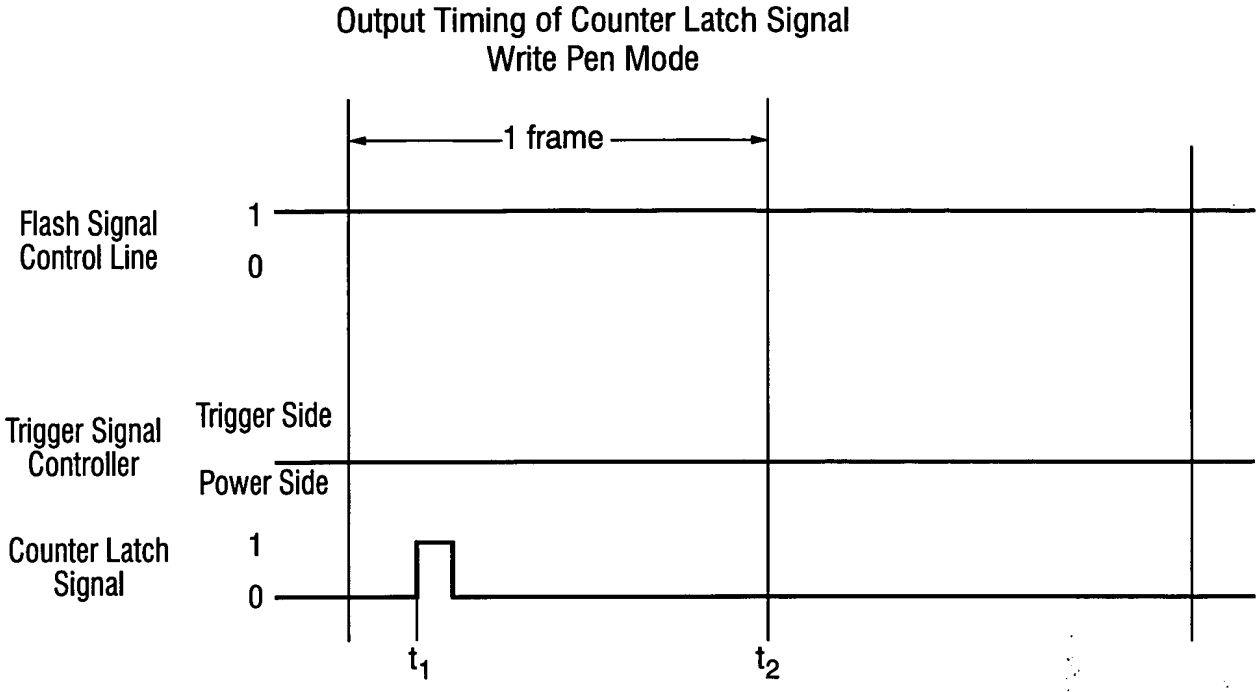


Fig. 14C

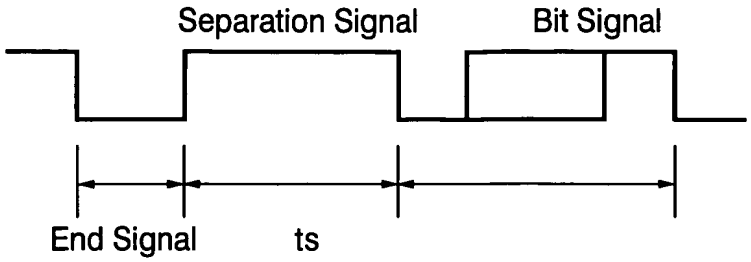


Fig. 15A

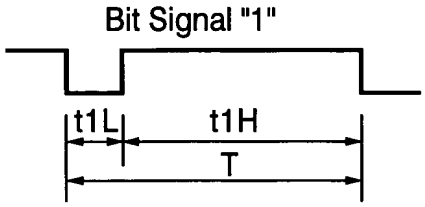


Fig. 15B

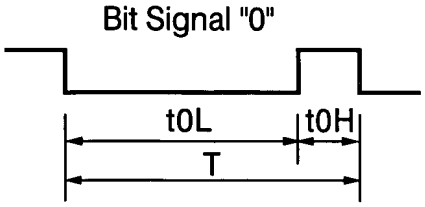


Fig. 15C

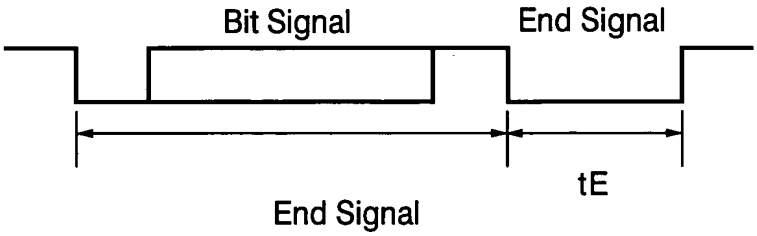


Fig. 15D

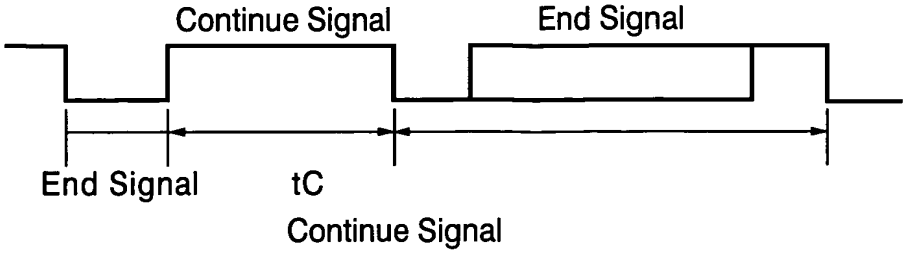
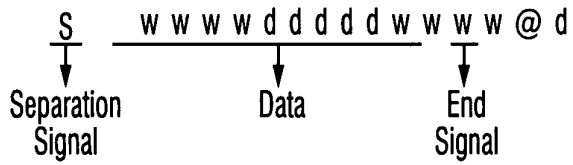
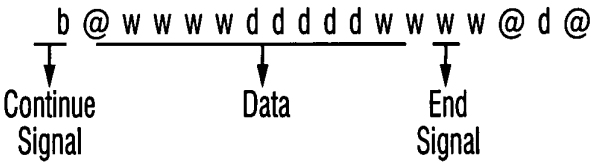


Fig. 15E



Command Frame

Fig. 16A



Response Frame

Fig. 16B

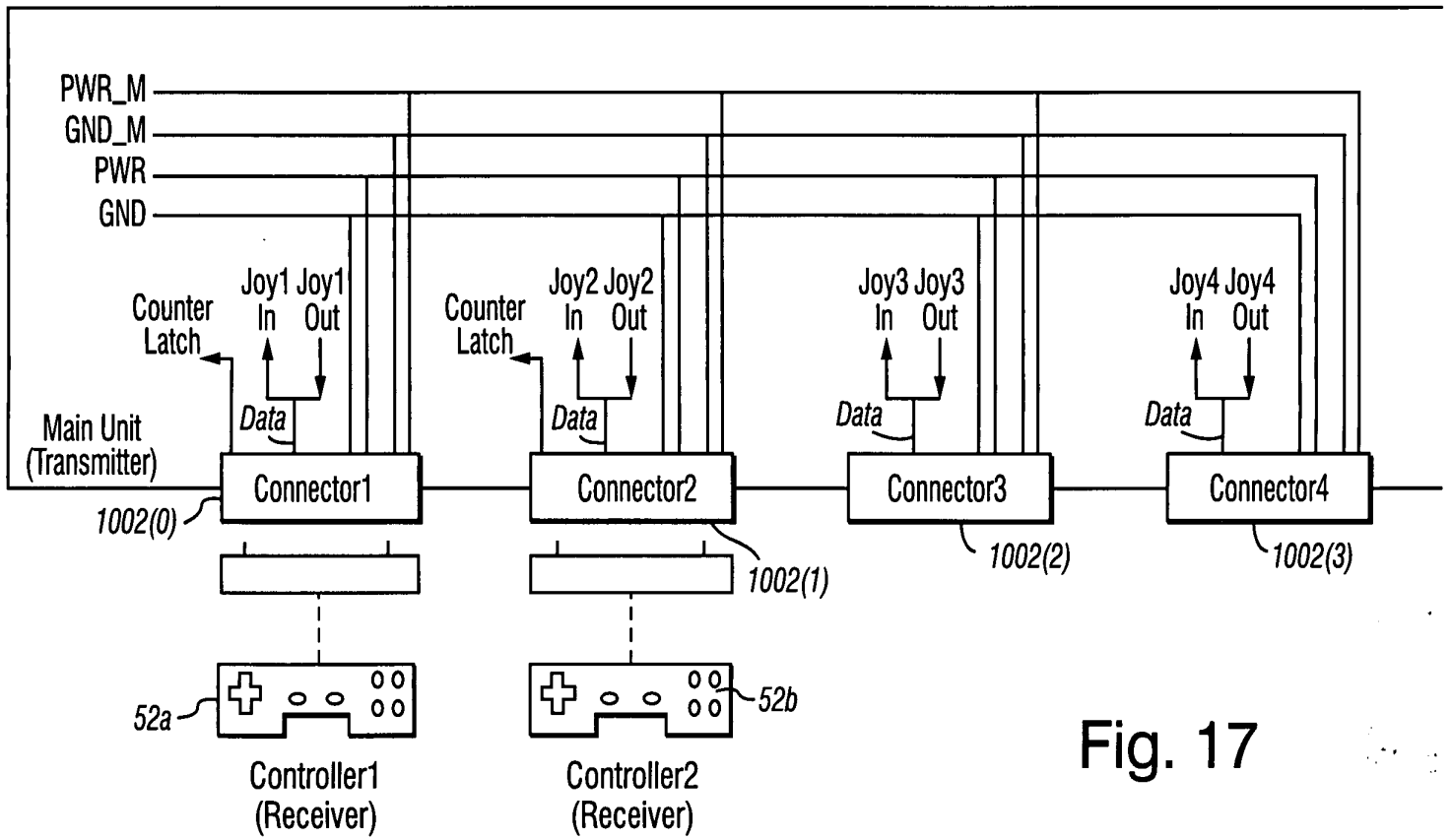


Fig. 17

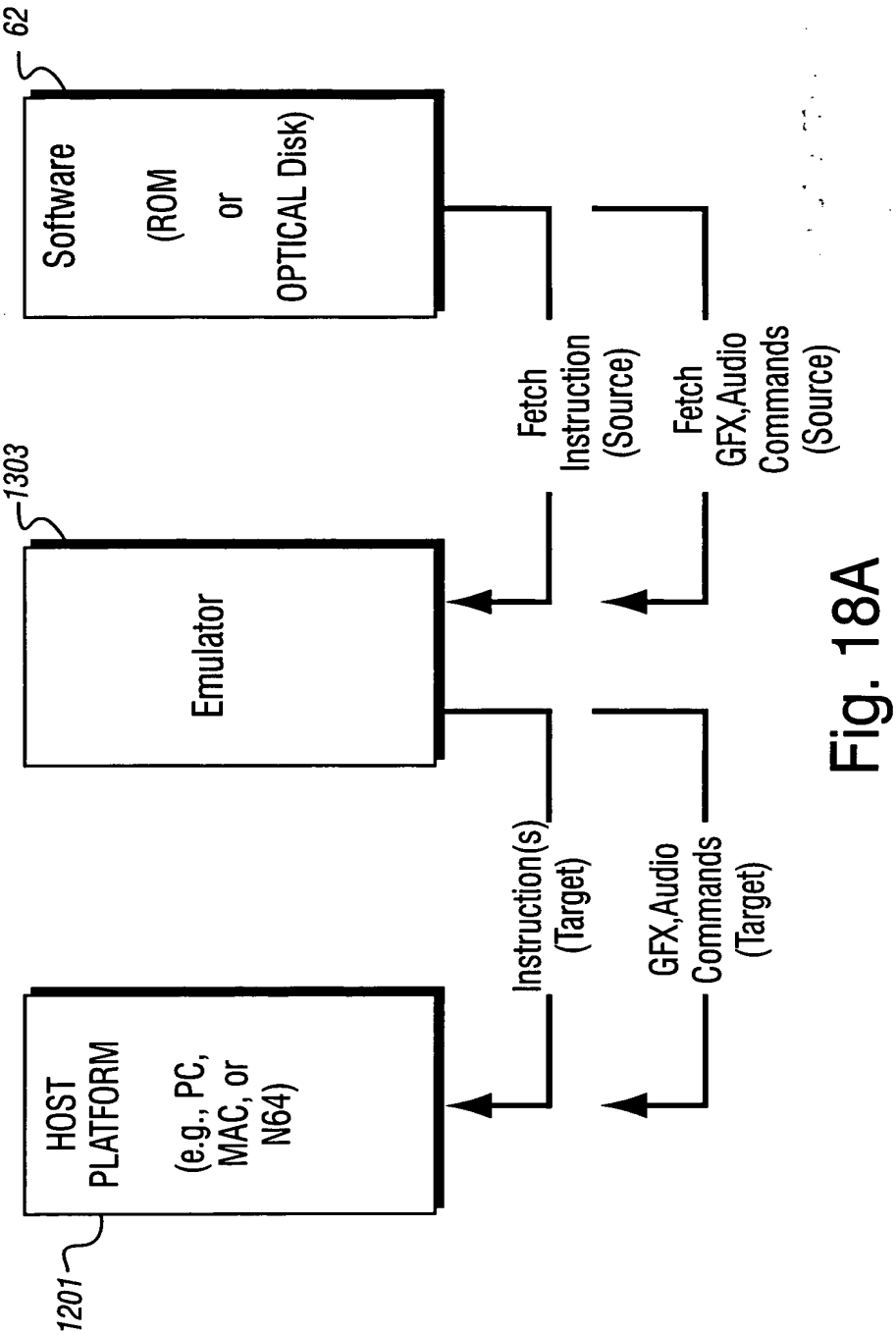


Fig. 18A

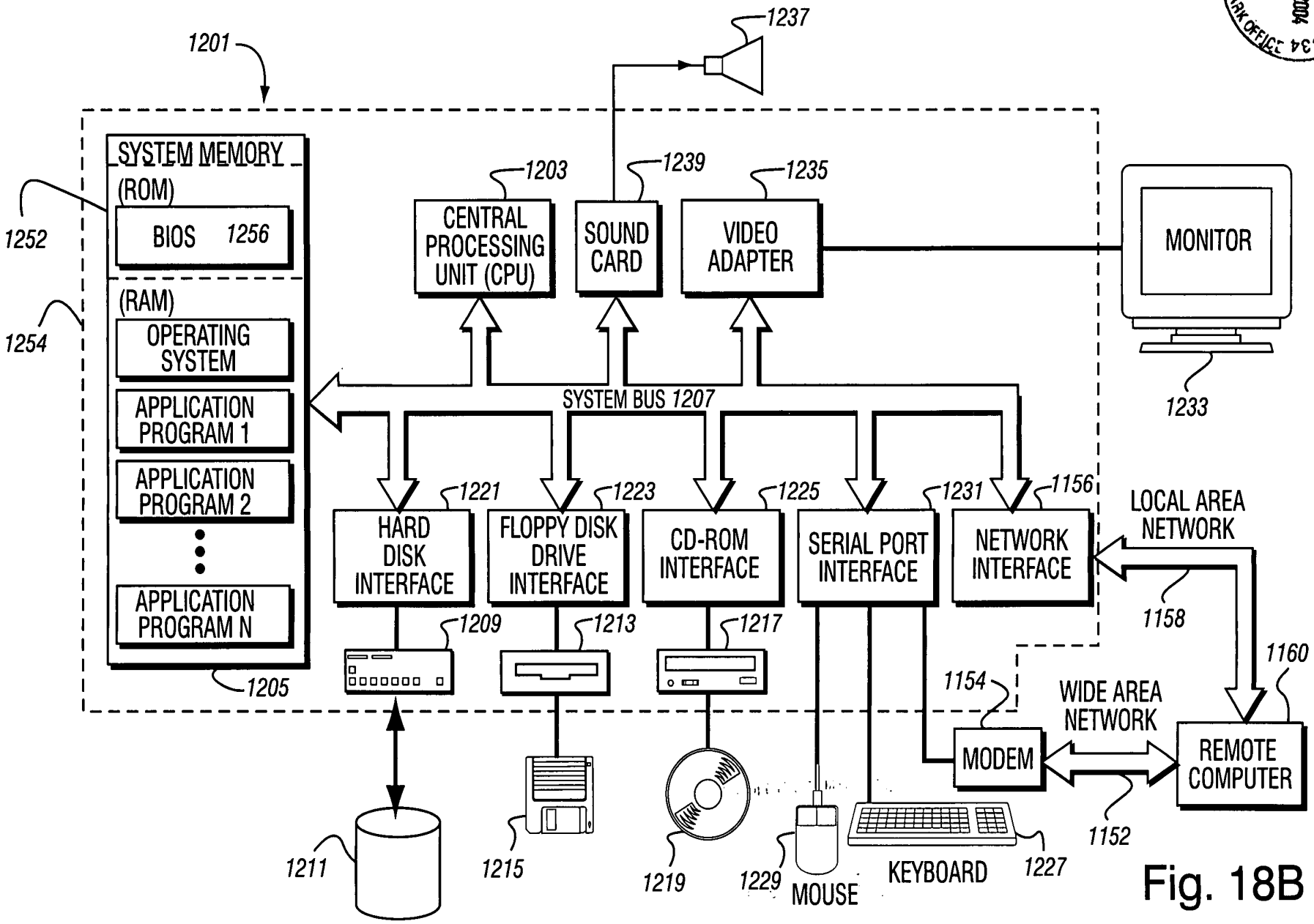


Fig. 18B